Description

Electronic transmitter/receiver

The invention relates to an electronic transmitter device as claimed in the preamble of claim 1, an electronic transmitter device as claimed in the preamble of claim 2, an electronic receiver device as claimed in the preamble of claim 22, an electronic receiver device as claimed in the preamble of claim 31 and an electronic receiver device as claimed in the preamble of claim 34.

In general terms, the invention relates to electronic telecommunications transmission systems in which data puncturing and/or data interleaving is carried out, or is at least partially carried out, at the transmitter end, and data de-interleaving and/or data depuncturing is carried out, or at least partially carried out, at the receiver end.

This takes place, for example, both within the scope of the HIPERLAN/2 (High Performance Radio Local Area Network Type 2) standard ("ETSI TS 101 761-1 Broadband Radio Access Networks; Hiperlan Type 2; Physical Layer") and within the scope of the standard "IEEE 802.11a - Part 11: Wireless LAN (WLAN) Medium Access Control and Physical Layer specifications: High-speed Physical Layer in the 5 GHz Band". In addition to said original standard, information on the HIPERLAN/2 standard can be obtained on the Internet at www.hiperlan2.com. A summary of the HIPERLAN/2 standard can also be found in the article "HIPERLAN type 2 for broadband wireless communication" by J. Khun-Jush et al. in Ericsson Review No. 2, 2000, pages 108 to 119.

In both of said standards a similar transmission fault

correction scheme is defined. It contains at the transmitter end (see fig. 2)

1) a convolutional coder 1 with the coding rate 1/2,

2) a first puncturing element P1 for reducing redundancy of 12 bits (only in the case of ETSI HIPERLAN/2),

3) a second puncturing element (P2) for selecting the coding rate (coding rates: 1/2, 9/16, 2/3, 3/4) and

4) an interleaver 2 for avoiding burst errors and, at the receiver end (see fig. 3), a corresponding de-interleaver 3 and corresponding depuncturing elements P2', P1'.

The puncturing process with the first puncturing element P1 is defined only in the ETSI standard mentioned above. The P2 rate of 2/3 occurs only in the IEEE standard mentioned above, the P2 rate of 9/16 occurs only in the ETSI standard. The following description relates essentially to said ETSI standard and to said IEEE standard. However, it is assumed to be generally quite clear that the present invention is not restricted to the application relating to the two said standards but rather can be applied generally to all transmitter/receiver devices in which the signal which is to be transmitted is punctured and/or interleaved after it has been coded and respectively de-interleaved and depunctured before it is decoded.

The coder 1 generates two parallel output bits for each input bit. The first puncturing element P1 removes a number of these output bits of the coder 1 according to a scheme in accordance with the following table 1. Where necessary, this puncturing scheme is applied to a group of 156 coded bits.

Table 1

Bit Numbering	**Puncturing pattern**	**Transmitted sequence (after parallel/serial conversion)**
0 - 155	X:1111110111111	X_0 Y_0 X_1 Y_1 X_2 Y_2 X_3 Y_3 X_4 Y_4
	Y:1111111111110	X_5 Y_5 X_7 Y_6 X_8 Y_7 X_9 Y_8 X_{10} Y_9 X_{11} Y_{10} X_{12} Y_{11}
> 156	X: 1	X_0 Y_0

or in the case of IEEE Y: 1

There is a difference in speed between the inputting and the outputting of the first puncturing element P1. For a group of 13 bits, for example, the coder 1 generates 2 x 13 bits, while the output of the first puncturing element P1 is 24 bits long. For this reason, in order to adapt the different speeds between the coding output and the puncturing output to one another, FIFO memory elements are provided in specific sections, for example upstream or downstream of the first puncturing element P1 or even upstream of the convolutional coder 1.

A particular feature of the standards mentioned above is that each possible data rate is assigned a specific form of modulation and a specific coding rate (for the channel coding). The assignment is selected in such a way that the number of the coded bits per OFDM (Orthogonal Frequency Division Multiplexing) symbol, referred to as NCBPS, is always a multiple of the number of subchannels (48 elements). Table 3 represents the specification of the transmission modes. It becomes clear that a BPSK (Binary Phase Shift Keying) modulation and a QPSK (Quaternary Phase Shift Keying) modulation as well as two amplitude modulations (16 QAM: 16-ary Quadrature Amplitude Modulation; 64 QAM: 64-ary Quadrature Amplitude Modulation) are used. The ratio of the number of uncoded bits to the number of coded bits is referred to as the coding rate r.

In the fastest mode (54 Mbps, 64 QAM), when both the first puncturing process P1 and the second puncturing process P2 (code rate 3/4) are applied, 222 input bits for an OFDM symbol must be coded (see table 3). For this reason, there would be 2 x 222 bits at the output of the coder1, and 1 x 432 bits at the

output of the first puncturing element P1.

According to the abovementioned standard definitions, the output data stream of the first puncturing element P1 is subjected again to serial/

parallel conversion (S/P) before it is fed to the second puncturing element P2.

The second puncturing element P2 again removes a number of the input bits, specifically according to the scheme illustrated in the following table 2.

Table 2

Code rates r	**Puncturing pattern**	**Transmitted sequence (after parallel/serial conversion)**
1/2	X: 1 Y: 1	X_0 Y_0
9/16 (only with ETSI)	X:111111110 X:111101111	X_0 Y_0 X_1 Y_1 X_2 Y_2 X_3 Y_3 X_4 X_5 Y_5 X_6 Y_6 X_7 Y_7 Y_8
2/3 (only with IEEE)	X: 11 Y: 10	X_0 Y_0 X_1
3/4	X: 110 Y: 101	X_0 Y_0 X_1 Y_2

The second puncturing process can be based on the same assumptions regarding the difference in speed as were made above for the first puncturing process. For this reason, an FIFO memory element is required again.

The serial output data stream of the second puncturing element P2 is finally transmitted to the interleaver 2 which re-orders the bits according to a double scheme. The interleaving is defined in accordance with a double scheme only within one OFDM symbol.

In what follows, k will be the index for the coded bit before the first permutation, i will be the index after the first permutation and before the second permutation, and j will be the index after the second

permutation directly before the assignment of modulation (the mapping).

The first permutation is defined by the following equation 1:

$$i = \frac{NCBPS}{16} \cdot (k \bmod 16) + \text{floor}\left(\frac{k}{16}\right) \qquad \text{(Eq. 1)}$$

where $k = 0, 1, \ldots, NCBPS-1$

The function floor(.) refers to the largest natural number which does not exceed the parameter, mod is the natural modulo operator, and NCBPS refers to the number of coded bits per OFDM symbol (NCBPS = Number of Coded Bits per OFDM Symbol).

The second permutation is defined by the following equation 2:

$$j = s \times \text{floor}\left(\frac{i}{s}\right) + \left(i + NCBPS - \text{floor}\left(16 \times \frac{i}{NCBPS}\right)\right) \bmod s \qquad \text{(Eq. 2)}$$

where $i = 0, 1, \ldots, NCBPS-1$

The value of s is determined by the number of coded bits per sub-carrier, NBPSC (= Number of Coded Bits Per Sub-Carrier) according to the following equation 3

$$s = \max\left(\frac{NBPSC}{2}, 1\right) \qquad \text{(Eq. 3)}$$

Table 3 combines the values of NBPSC and NCBPS for the various transmission modes with NUBPS (= Number of Uncoded Bits Per OFDM Symbol),

specifically both for the case in which the first puncturing element P1 which is illustrated in fig. 1 is used and for the case in which the first puncturing element P1 is not applied.

Table 3: Main parameters for various transmission modes

Transmission mode (type of modulation and coding rate)	**N_{BPSC}**	**N_{UBPS} P1 not applied**	**N_{UBPS} P1 applied**	**N_{CBPS}**	**Interleaver operation mode**
BPSK 1/2	1	24	26	48	0
BPSK 3/4	1	36	39	48	0
QPSK 1/2	2	48	52	96	1
QPSK 3/4	2	72	78	96	1
16 QAM 1/2	4	96	102	192	2
16 QAM 9/16	4	108	112	192	2
16 QAM 3/4	4	144	150	192	2
64 QAM 2/3	6	192	198	288	3
64 QAM 3/4	6	216	222	288	3

The inverse functions must be carried out at the receiver end (fig. 3). In this case, each bit is assigned a reliability measure for the Viterbi decoder 4 which is represented by N-1 bits. It is possible to state that each bit is represented by N soft bits, one soft bit being one word (see fig. 11).

In the depuncturing function, soft zeros are inserted in the received data stream where bits had been removed at the transmitter end. This is carried out downstream of the de-interleaver output according to tables 4 and 5 correspondingly by means of the first depuncturing element P2' which corresponds in its method of operation to a reversal of the second puncturing element P2, and by means of the second

depuncturing element P1' which corresponds in its method of operation to a reversal of the first puncturing element P1.

Table 4: Depuncturing scheme of the first depuncturing element P2'

Coding Rate r	**Received sequence**	**Output sequence**
1/2	X_0 Y_0	X: X_0 Y: Y_0
9/16	X_0 Y_0 X_1 Y_1 X_2 Y_2 X_3 Y_3 X_4 X_5 Y_5 X_6 Y_6 X_7 Y_7 Y_8	X: X_0 X_1 X_2 X_3 X_4 X_5 X_6 X_7 0 Y: Y_0 Y_1 Y_2 Y_3 0 Y_5 Y_6 Y_7 Y_8
2/3	X_0 Y_0 X_1	X: X_0 X_1 Y: Y_0 0
3/4	X_0 Y_0 X_1 Y_2	X: X_0 X_1 0 Y: Y_0 0 Y_2

Table 5: Depuncturing scheme of the second depuncturing element P1'

Bit numbering	**Received sequence**	**Output sequence**
0 - 155	X_0 Y_0 X_1 Y_1 X_2 Y_2 X_3 Y_3 X_4 Y_4 X_5 Y_5 X_7 Y_6 X_8 Y_7 X_9 Y_8 X_{10} Y_9 X_{11} Y_{10} X_{12} Y_{11}	X: X_0 X_1 X_2 X_3 X_4 X_5 0 X_7 X_8 X_9 X_{10} X_{11} X_{12} Y: Y_0 Y_1 Y_2 Y_3 Y_4 Y_5 Y_6 Y_7 Y_8 Y_9 Y_{10} Y_{11} 0
> 156	X_0 Y_0	X: X_0 Y: Y_0

As at the transmitter end, the same problems also arise here in terms of latency and speed adaptation.

Let us concentrate now on the first permutation (Equation 1). In table 6, the 288 input/output bits for the 64 QAM mode are illustrated.

Table 6

Mode #3		Mode #3		Mode #3		Mode #3		Mode #3		Mode #3	
k	i	k	i	k	i	k	i	k	i	k	i
0	0	48	3	96	6	144	9	192	12	240	15
1	18	49	21	97	24	145	27	193	30	241	33
2	36	50	39	98	42	146	45	194	48	242	51
3	54	51	57	99	60	147	63	195	66	243	69
4	72	52	75	100	78	148	81	196	84	244	87
5	90	53	93	101	96	149	99	197	102	245	105
6	108	54	111	102	114	150	117	198	120	246	123
7	126	55	129	103	132	151	135	199	138	247	141
8	144	56	147	104	150	152	153	200	156	248	159
9	162	57	165	105	168	153	171	201	174	249	177
10	180	58	183	106	186	154	189	202	192	250	195
11	198	59	201	107	204	155	207	203	210	251	213
12	216	60	219	108	222	156	225	204	228	252	231
13	234	61	237	109	240	157	243	205	246	253	249
14	252	62	255	110	258	158	261	206	264	254	267
15	270	63	273	111	276	159	279	207	282	255	285
16	1	64	4	112	7	160	10	208	13	256	16
17	19	65	22	113	25	161	28	209	31	257	34
18	37	66	40	114	43	162	46	210	49	258	52
19	55	67	58	115	61	163	64	211	67	259	70
20	73	68	76	116	79	164	82	212	85	260	88
21	91	69	94	117	97	165	100	213	103	261	106
22	109	70	112	118	115	166	118	214	121	262	124
23	127	71	130	119	133	167	136	215	139	263	142
24	145	72	148	120	151	168	154	216	157	264	160
25	163	73	166	121	169	169	172	217	175	265	178
26	181	74	184	122	187	170	190	218	193	266	196
27	199	75	202	123	205	171	208	219	211	267	214

28	217	76	220	124	223	172	226	220	229	268	232
29	235	77	238	125	241	173	244	221	247	269	250
30	253	78	256	126	259	174	262	222	265	270	268
31	271	79	274	127	277	175	280	223	283	271	286
32	2	80	5	128	8	176	11	224	14	272	17
33	20	81	23	129	26	177	29	225	32	273	35
34	38	82	41	130	44	178	47	226	50	274	53
35	56	83	59	131	62	179	65	227	68	275	71
36	74	84	77	132	80	180	83	228	86	276	89
37	92	85	95	133	98	181	101	229	104	277	107
38	110	86	113	134	116	182	119	230	122	278	125
39	128	87	131	135	134	183	137	231	140	279	143
40	146	88	149	136	152	184	155	232	158	280	161
41	164	89	167	137	170	185	173	233	176	281	179
42	182	90	185	138	188	186	191	234	194	282	197
43	200	91	203	139	206	187	209	235	212	283	215
44	218	92	221	140	224	188	227	236	230	284	233
45	236	93	239	141	242	189	245	237	248	285	251
46	254	94	257	142	260	190	263	238	266	286	269
47	272	95	275	143	278	191	281	239	284	287	287

From table 6 it is clear that if the input bits are written in columns into a matrix with 16 rows and 18 columns, the bits can then be read in rows from the top in the correct sequence. In addition, said column size 18 is precisely three times the bit number per carrier, or in other words precisely the magnitude which is required to carry out the second permutation. It is also possible to show that precisely the same principle can be applied to the other modes. It is sufficient to reduce the number of columns correspondingly to 12, 6 or 3 for 16 QAM, QPSK or BPSK.

The principle of the first permutation is summarized in fig. 4. With the described method of execution,

up to 288 cycles are required to write the contents of one complete OFDM symbol.

In summary it is therefore possible to state the following with respect to the prior art:

1) The delay which is introduced by the system according to the prior art is high since for puncturing a bit number is required which is twice as high as the number of input bits (maximum 432 cycles/OFDM symbol), and since all the input bits have to be read serially for interleaving (maximum 288 cycles/OFDM symbol). The latency is a critical parameter for the configuration of burst transmission systems such as, for example, WLAN.
2) FIFO elements are required in order to compensate the speed differences between the coder 1 and the first puncturing element P1 and between the first puncturing element P1 and the second puncturing element P2. In addition, FIFO elements are required in order to compensate the speed difference between the parallel inputting of the second puncturing element P2 and the serial inputting of the interleaver 2.
3) The clock system has to be fast enough in order to be able to conclude everything within one OFDM symbol. In an implementation with a clock frequency of 80 MHz, two OFDM symbols, and consequently two bit bursts which are supplied to the coder 1, are 3.6 µs * 80 MHz = 288 clock cycles away from one another (worst case with short guard interval with HIPERLAN; typical case: 4.0 µs * 80 MHz = 320 clock cycles). During this time, the input data must be read and stored somewhere. After this, it has to be read out in the correct sequence (Equation 1) and the second permutation (Equation 2) has to be carried out. The puncturing elements P1, P2

and the interleaver 2 take up to 432 clock cycles in order to read all the input bits. For this reason it is not possible to complete all the operations within one OFDM symbol, for which reason, according to the prior

art, what are referred to as pipelines are produced for even-numbered and odd-numbered OFDM symbols by doubling the circuit or even multiplying it further.

The invention is therefore based on the object of making available electronic transmitter devices having a puncturing device and/or an interleaver, electronic receiver devices having a de-interleaver and/or a depuncturing device, and a telecommunications transmission system having a puncturing device and/or an interleaver and/or a de-interleaver and/or a depuncturing device, which overcome the speed difference problems during data processing which have been explained above with respect to the prior art.

This object is achieved according to the invention by means of an electronic transmitter device as claimed in claim 1, by means of an electronic transmitter device as claimed in claim 2, by means of an electronic receiver device as claimed in claim 22, by means of an electronic receiver device as claimed in claim 31, by means of an electronic receiver device as claimed in claim 34 and by means of a telecommunications transmission system as claimed in claim 41.

The speed differences which are present according to the prior art are overcome with the devices according to the invention by means of the parallelization of the data streams.

The term "telecommunications transmission system" is to be understood quite generally as a system for transmitting any desired information, i.e. for example language, images, data etc.

Advantageous and preferred embodiments of the electronic transmitter device according to the invention as claimed in claim 1 are the subject matter of claims 4 to 21. Advantageous and preferred embodiments of the electronic transmitter device according to the invention as claimed in claim 2 are the subject matter of claims 3 and 5 to 12. Advantageous and preferred embodiments of the electronic receiver device according to the invention as claimed in claim 22 are the subject matter of claims 23 to 30. Advantageous and preferred embodiments of the electronic receiver device according to the invention as claimed in claim 31 are the subject matter of claims 32 to 33. Advantageous and preferred embodiments of the electronic receiver device according to the invention as claimed in claim 34 are the subject matter of claims 35 to 40. Advantageous and preferred embodiments of the telecommunications transmission system according to the invention are the subject matter of claims 42 to 45.

Exemplary embodiments of the invention are explained below with reference to the figures, in which:

fig. 1 shows an exemplary embodiment of a transmitter device according to the invention,

fig. 2 shows a transmitter device according to the prior art,

fig. 3 shows a receiver device according to the prior art,

fig. 4 shows the principle of the first permutation,

fig. 5 shows an execution scheme for the execution of a first puncturing process according to the invention,

fig. 6 shows an exemplary embodiment of the circuit of a first puncturing element according to the invention,

fig. 7 shows the time sequence diagram associated with

the circuit in fig. 6,

fig. 8 shows an execution scheme for the execution of a second puncturing process according to the invention,

fig. 9 shows an exemplary embodiment of the circuit of a second puncturing element according to the invention,

fig. 10 shows the time sequence diagram which is associated with the circuit in fig. 9,

fig. 11 shows an exemplary embodiment of a receiver device according to the invention,

fig. 12 shows an example of a depuncturing function in accordance with the invention for the coding rate 3/4,

fig. 13a shows an exemplary embodiment of the circuit of a first depuncturing element according to the invention,

fig. 13b shows an exemplary embodiment of the circuit of a second depuncturing element according to the invention,

fig. 14 shows examples of the first depuncturing function in accordance with the invention for various coding rates,

fig. 15 shows a modified bit mapping,

fig. 16 shows an exemplary embodiment of an interleaver according to the invention with registers,

fig. 17 shows a re-ordering scheme of the memory element in the interleaver,

fig. 18 is a schematic view of a writing phase of the first permutation in the interleaver for an exemplary embodiment of the interleaver with an RAM,

fig. 19 is a schematic view of a reading phase of the first permutation in the interleaver for an exemplary embodiment of the interleaver with an RAM,

fig. 20 is a schematic view of an exemplary embodiment of the writing phase during the inversion of the first permutation in the de-interleaver, and

fig. 21 is a schematic view of an exemplary embodiment of the reading phase during the inversion of the first permutation in the de-interleaver.

It is possible to reformulate the equations defined in the abovementioned standards in such a way that the

entire data path can be processed in two parallel lines. Fig. 1 shows a corresponding block circuit diagram for the transmitter end.

From fig. 5 it is apparent that the first puncturing which is to be carried out by the first puncturing element P1 can be implemented in a parallel fashion. If the parallel outputs Out_X and Out_Y are read alternately, the original sequence is obtained. The only difference is that in this case there is also an empty location which lies precisely in the center, in terms of the timing, during the output sequence of fig. 5. The hardware block which follows the first puncturing element, i.e. the second puncturing element P2, must be informed by means of a signal, referred to below as "data_valid signal", that it is not intended to include the empty location.

In the fastest mode with 222 input bits, the coder 1 generates 2 × 222 bits, and the output length remains 2 × 222 (with 2 × 6 gaps). One possible way of implementing the described method of operation in terms of hardware is the circuit illustrated in fig. 6.

In the circuit in fig. 6, the first data input IN_X of the first puncturing element P1 which is illustrated there is connected via a first 1-step delay register D to the first data output Out_X of the first puncturing element P1 (upper data line in fig. 6). The lower data line of fig. 6 shows the logic linking of the second data input IN_Y of the first puncturing element P1 with its second data output Out_Y. The essential element in this connection is a multiplexer MUX at whose first input the data which is incoming into the first puncturing element P1 via the second data input IN_Y of the first puncturing element P1 is made available after passing through a 1-step delay register D. In parallel with this, the data which is incoming into the first puncturing element P1 via the second data input IN_Y of the first puncturing element P1 is also fed directly to a second input of the multiplexer MUX.

The multiplexer MUX has an output which is electrically connected to the second data output Out_Y of the first puncturing element P1 via a further 1-step delay register D.

As is readily apparent, in the circuit example according to fig. 6 it is possible to select when the bit pair is to be removed by suitably setting the multiplexer MUX and suitably setting up the 1-step delay registers D. fig. 7 shows the corresponding time sequence diagram. The data bits of an OFDM symbol (222) are transmitted in a single burst to the convolutional coder 1. The latter generates a burst of the same length on two parallel lines. The first puncturing element P1 re-orders the two coding outputs and signals the positions of the six gaps to the second puncturing element P2 by setting the data_valid signal to LOW.

FIFO memory elements are no longer required with such transmitter devices according to the invention because the coder 1 and the puncturing units P1, P2 which have the first puncturing element P1 and the second puncturing element P2, operate at the same speed. In addition, the time required to execute the transmitter-end processing operation is greatly reduced (222 cycles). For this reason, when applying the invention it is possible to use a single structure with a clock frequency of 62 MHz instead of 120 according to the prior art, that is to say "pipelines" are no longer required.

It is then possible to apply the same principle to the second puncturing element P2. In fig. 8, all the possible puncturing schemes are illustrated, but the coding rate 1/2 is absent because this means "do nothing". The latency which is introduced by this unit, that is to say by the second puncturing element P2, is

again equal to one clock cycle, while the time which is necessary to execute the operation

corresponds to the number of input data bits (222 at maximum).

Fig. 9 shows an example of an inventive implementation of the second puncturing element P2. In the circuit illustrated in fig. 9, the second puncturing element P2 has three multiplexers MUX, each of which has in turn two inputs and one output and is also connected to a control line mux_0, mux_1.

The first data input IN_X of the second puncturing element P2 is directly electrically connected both to the first input of the first multiplexer of the second puncturing element P2 and to the first input of the second multiplexer of the second puncturing element P2. The second data input IN_Y of the second puncturing element P2 is directly electrically connected both to the second input of the first multiplexer of the second puncturing element P2 and to the second input of the second multiplexer of the second puncturing element P2.

The output of the first multiplexer of the second puncturing element P2 is directly electrically connected to the first input of the third multiplexer of the second puncturing element P2. In parallel with this, the output of the first multiplexer of the second puncturing element P2 is also electrically connected via a 1-step delay register D to the second input of the third multiplexer of the second puncturing element P2.

The output of the third multiplexer of the second puncturing element P2 is electrically connected via a 1-step delay register D to the first data output Out_X of the second puncturing element P2. The output of the second multiplexer of the second puncturing element P2 is electrically connected via a further 1-step

delay register D to the second data output Out_Y of the second puncturing element P2.

From fig. 9 it becomes clear that the desired output sequences can easily be achieved by suitably controlling the multiplexers MUX and suitably setting up the 1-step delay registers D.

In the timing diagram (illustrated in fig. 10) for the second puncturing process, the first part of the outputting is expanded according to fig. 7. The outputting of the second puncturing element P2 for the 3/4 rate is illustrated in fig. 10. The gaps which have already been introduced by the first puncturing element P1 remain in the same position, but the newly introduced gaps are also shown. The data_valid signal is set for both types of gaps LOW.

Finally, the interleaver 2 must also be configured in such a way that it is capable of processing two parallel inputs instead of 1. However, before this is described in more detail below, the new method of depuncturing at the receiver end will firstly be treated.

The inventive method of depuncturing at the receiver end functions in principle in precisely the same way as the inventive method of puncturing at the transmitter end. Fig. 11 shows a corresponding block circuit diagram with de-interleaver 3, first depuncturing element P2', second depuncturing element P1' and Viterbi decoder 4. In fig. 12, the depuncturing function for the coding rate 3/4 is illustrated, soft zeros being inserted in place of the missing bits. It is a precondition here that the de-interleaver 3 is already capable of inserting gaps at the end of a depuncturing group. The de-interleaver 3 therefore already carries out the FIFO function in order to

adapt the various input/output speeds to one another, and there is no need for an additional separate memory. For more precise statements in this respect, reference is made to the explanations given below which relate to the inventive method of operation of the de-interleaver 3.

Even if the first puncturing element P1 is also used, the de-interleaver 3 must ensure that a gap is also left at the end of a first puncturing group. The first depuncturing element P2' firstly fills in the gaps which are associated with the second puncturing group, and finally the second depuncturing element P1' fills in the remaining gaps. All the bursts in each section have a length which is equal to the number of uncoded bits. For this reason, the latency for the first depuncturing element P2' has one cycle, and one further cycle for the second depuncturing element P1'.

A case with the 3/4 rate was illustrated in fig. 12 but the principle can also be expanded to all other coding rates. This is shown for the first depuncturing element P2' in fig. 14.

An example of a hardware implementation of the first depuncturing element P2' is illustrated in fig. 13a, and fig. 13b shows an example of a hardware implementation of the second depuncturing element P1'. In the circuit according to fig. 13a/13b, the inputting/outputting is represented by N soft bits for the following Viterbi decoder 4.

In the exemplary embodiment of the first depuncturing element P2' according to fig. 13a, the first depuncturing element P2' has a first and a second multiplexer MUX, each with two inputs and one output, as well as a third multiplexer MUX with four inputs and one output.

In each case a 1-step delay register D is connected between the output of the first multiplexer and one input of the second multiplexer, between the output of the second multiplexer and a first data output Out_X of the first depuncturing element P2', between the output of the third multiplexer and a second data output Out_Y of the first depuncturing element P2', and between a first data input IN_Y of the first depuncturing element P2' and an input of the third multiplexer.

The first data input IN_Y of the first depuncturing element P2' is also directly electrically connected to an input of the first multiplexer and to a further input of the third multiplexer. The second data input IN_X of the first depuncturing element P2' is directly electrically connected to the further input of the second multiplexer and to the third input of the third multiplexer. The respectively remaining input of the first multiplexer and of the third multiplexer is connected to a line on which soft zeros are made available.

In the exemplary embodiment of the second depuncturing element P1' according to fig. 13b, the second depuncturing element P1' has three multiplexers MUX, each with two inputs and one output. In each case a 1-step delay register D is connected between the output of the first multiplexer and an input of the second multiplexer, between the output of the second multiplexer and the first data output Out_X of the second depuncturing element P1', and between the output of the third multiplexer and the second data output Out_Y of the second depuncturing element P1'. The first data input IN_X of the second depuncturing element P1' is directly electrically connected to an input of the first multiplexer and to the further input of the second multiplexer. The second data input IN_Y

of the second depuncturing element P1' is directly electrically connected to an input of the third multiplexer. The respectively remaining input of the first multiplexer and of the third multiplexer is connected to a line on which soft zeros are made available.

From figs 13a and 13b it becomes apparent that the desired output sequences can easily be achieved by suitably controlling the multiplexers MUX and suitably setting up the 1-step delay registers D.

There will now be a more precise description of exemplary embodiments of the interleavers 2 and de-interleavers 3 in the transmitter/receiver devices according to the invention.

Reference is made to fig. 1 with respect to the transmitter-end position of the interleaver 2. It will also be recalled that the second puncturing element P2 is capable of making available the even-numbered bit according to Equation 1 at its first data output Out_X, and the odd-numbered bits according to Equation 1 at its second data output Out_Y.

In order to explain exemplary embodiments of interleavers according to the invention, two new possible implementations of the first permutation scheme will be illustrated in what follows. The first implementation is realized using registers, and understanding of the first implementation is useful in order to understand the second implementation possibility, explained further below, by means of an RAM.

Firstly, the column carrier diagram in fig. 4 is modified so that the new diagram according to fig. 15 is produced. The result of this is that the three groups

of six rows are always associated with the same carriers independently of the selected transmission mode.

Fig. 16 shows, as an example, an interleaver embodiment with registers. This exemplary embodiment according to fig. 16 contains two rows of 8-bit shift registers. The second puncturing element P2 provides the interleaver 2 with even-numbered bits (Out_X) and odd-numbered bits (Out_Y) which are shifted within the even-numbered/odd-numbered register group. After 2 × 8 inputs, the registers are full. It is then possible to shift a complete column of the matrix of the matrix register which is present in addition to the shift registers and which is a 16 × 18 matrix register in the present exemplary embodiment, and then start again with the filling of the even-numbered/odd-numbered shift registers. Depending on the selected mode, the columns (0, 12, 6) ... (0, 1, 2 ..., 17) are each correspondingly written for BPSK...64 QAM. For the 64 QAM mode, the phase of writing into the matrix register requires 18 (number of columns) × 8 (required time for filling the shift registers) = 144 cycles. Consequently, this time is halved in comparison with the time which is required for the serial implementation which is specified in the abovementioned standards.

For the reading phase, the matrix rows then have to be read. A row always contains the bits which are required to map the three QAM carriers. It is possible to apply the second permutation (Equation 2) to the complete row once, or to execute the same permutation on the three carriers serially three times. The reading phase correspondingly lasts either for 16 or 48 cycles. The total time which is required for the interleaving in the last-mentioned case is 144 + 48 = 192 cycles. For

this reason, only a single interleaver 2 with a clock frequency of higher than 53.3 MHz has to be used. In the example mentioned with a clock frequency of 80

MHz, 96 cycles are still free. These free cycles may be used for the case in which the puncturing device P1, P2 makes available the input bits with gaps between them. This is precisely the case which has already been described with respect to the above exemplary embodiment of the puncturing device P1, P2 according to the invention, in which the data which is input at the interleaver 2 is distributed over 222 cycles. The entire interleaving time is then 270 cycles long, the minimum clock frequency at which pipelines can be avoided being 75 MHz.

Taking as a starting point the exemplary embodiment of the interleaver which has just been described, and has registers, the memory elements can be re-ordered in such a way that it is possible to obtain a more suitable configuration for an RAM implementation of the interleaver 2. With respect to the illustration in fig. 16, it is to be noted that the left-hand block of the matrix register is firstly written to, the central block is written to secondly, and finally the right-hand block is written to last. These three blocks are then written to in columns in the aforesaid sequence (see fig. 17).

In order to write the two bits which come from the puncturing unit P1, P2 it is necessary to access two rows (or one column) in a cycle. However, with a standard RAM it would be desirable only to access one row per cycle. For this reason, each block is further divided into two columns, one with the even-numbered rows and the second with the odd-numbered rows (see fig. 17). As a result, the even-numbered bit and the odd-numbered bit which come from the puncturing unit P1, P2 are now on the same row and they can be written simultaneously in a single cycle. Finally, an RAM block with 24 rows and 12 columns is obtained, as shown in fig. 18. The 64 QAM case is explained below. Taking this as a basis, the expansion to the other modes is then uncomplicated.

It must be possible to write precisely 2 bits into one row of 12 (for example RAM with individual bit writing). At first, we shall concentrate on the first block of 8 rows (that is the left-hand block in the register implementation in fig. 16). At first, rows are written to from 0 to 7, and the columns 0 and 6 are always written to. In this way, the first 2 x 8 bits are written to. The rows 0 to 7 are then written to, but this time the columns 1 and 7 etc. up to the bits 94, 95 are always written to. Now, the block of rows is changed and the rows from 8 to 15 are considered, and everything is repeated up to the bit 191. Then, the block is changed for the last time, and the rows from 16 to 23 up to the last bit are processed (see fig. 18).

The bits then have to be read in the correct sequence and thus prepared for the second permutation. It is easy to see that the groups of 6 bits have to be fetched from the memory in the sequence illustrated in fig. 19.

Consequently, the rows with the following addresses have to be read: 0, 8, 16, 0, 8, 16, 1, 9, 17, 1, 9, 17, ..., 23. The 6 MSB (MSB = Most Significant Bits, bits located on the left) are extracted three times from the 12 bits and the same second permutation scheme is applied. The next time, the 6 LSB (LSB - Least Significant Bits, bits on the right) are extracted and the subsequent second permutation scheme is applied.

As stated above, the explained example relates to the 64 QAM case. It is easy to check that the permutation fills the stated requirements. In addition it is easy to transfer the explained system to BPSK, QPSK and 16 QAM. All that is necessary is to reduce the number of columns during the writing phase, in each case accordingly to the

columns (0, 6), (0...1, 6...7) and (0...3, 6...9).

In summary, the advantage of the RAM embodiment of the interleaver 2 with respect to the register embodiment of the interleaver 2 is that in the RAM embodiment the data bits are not buffered in shift registers but instead the bit pairs are written directly into the RAM at the correct addresses.

As already described above with respect to the depuncturing unit (P2', P1'), also at the receiver end, the standard solution is reconfigured to form a completely parallel solution, as illustrated in the block circuit diagram in fig. 11. The demapper unit, which is arranged upstream of the de-interleaver 3, supplies the de-interleaver 3 with one carrier per cycle. Each carrier contains 1, 2, 4 or 6 soft bits corresponding to the selected modulation mode (mapping as in fig. 15). A soft bit is equal to the specific bit plus N-1 reliability bits which have to be processed together up to the Viterbi decoder 4, whose output is a single specific bit. For this reason, in this case, the basic data element is no longer the bit but rather a group of N bits, N typically being equal to 4. At the receiver end, the RAM solution is the preferred embodiment because the necessary memory elements are increased by a factor N. Here too, there is no need for buffering of the (output) bits into (output) shift registers with the RAM solution but instead the bits are read out of the RAM in pairs directly into the depuncturing device (P2', P1').

At the receiver end, the second and the first permutation are carried out inversely.

After the inverse of the second permutation has been carried out, each carrier (group of 1, 2, 4 or 6 soft bits corresponding to the modes BPSK, QPSK, 16 QAM or 64 QAM) moves on to carrying out the inverse of the first permutation. Here, it is possible in turn to use an RAM with 24 rows of 12 x N bits. The writing phase follows the same scheme as the reading phase at the transmitter end and is illustrated in fig. 20. The reading phase is shown in fig. 21 and follows the same scheme as the writing phase at the transmitter end.

The total time which is required to carry out the de-interleaving of an OFDM symbol is 48 cycles for the writing phase for all transmission modes + 144 cycles for the reading phase with 64 QAM. In order to facilitate the operation of the depuncturing unit (P2', P1') which is connected downstream of the de-interleaver 3 it is possible to leave a number of gaps between the data during the reading phase (222 cycles). For further details in this respect, reference is made to the above statements on the depuncturing device (P2', P1').

It is just as simple, as has been explained above with respect to the RAM implementation, to implement at the receiver end an inversion of the interleaver register implementation as an exemplary embodiment according to the invention. The data input process, as explained with respect to the register example of the interleaver 2, only has to be reversed into a data output process. At the receiver end, a soft bit column is then read, interleaved in the manner of a comb, from the matrix register into two soft bit shift registers, i.e. two adjacent soft bits are each read into another of the two soft bit shift registers. From the two soft bit shift registers, the outputting of soft bits into the depuncturing device (P2', P1') is respectively carried out in a serial fashion, but in an overall parallel

fashion owing to the presence of two soft bit shift registers. As soon as the two soft bit shift registers are empty, a further column is read out from the matrix register into both soft bit shift registers in the same way as in the first column which is read out from the matrix register, and then both soft bit shift registers are simultaneously emptied, and so on.

In terms of hardware, in one exemplary embodiment of the de-interleaver 3 the matrix register is embodied, for example as a 16 × (18 × N) matrix register, and the two soft bit shift registers are embodied as 8 soft bit shift registers with a word length of N.

In summary, the advantages which are achieved with the solution according to the invention can be summarized as follows:

1) A reduction in delay at the transmitter and at the receiver. The latency or delay is usually a particularly critical parameter for the configuration of a burst transmission system. The latency which is reduced in the puncturing device/depuncturing device P1, P2, P2', P1' and in the interleaver/de-interleaver 2, 3 can consequently be included advantageously in other parts of the burst transmission system, for example in the equalizer or in the synchronization means, in order to be able to implement more powerful algorithms there.
2) A reduction in the space required since a FIFO is no longer required.
3) Furthermore, low clock frequencies are also associated with this. If a WLAN system is implemented with a clock of 80 MHz, i.e. four times the OFDM sampling frequency, according to the invention the data path no longer has to be

doubled into odd-numbered/even-numbered OFDM symbols as is necessary according to the prior art.

If one of the exemplary embodiments illustrated above is used at the transmitter end for the transmitter device according to the invention, and one of the exemplary embodiments illustrated above is used at the receiver end for the receiver device according to the invention, an exemplary embodiment for a telecommunications transmission system according to the invention is obtained which may be, for example, a WLAN.